

S6: (1) "9213802"  
 S12: (1) "09213802"  
 S13: (1) "11168199"  
 S14: (7374) transistor and ((interlayer near2 (insulat\$  
 S15: (1356) S14 and (second adj gate)  
 S16: (152) S15 and (second adj (sidewall or (side adj w  
 S17: (157) S16 and (conduct\$4)  
 S18: (36) S17 and ((driv\$4 or control\$4) near2 transist  
 S19: (3) Backward citation search 7  
 S20: (20) Forward citation search 6  
 S22: (101) S17 not (S18 S19 S20)  
 S23: (101) S22 and (second adj (sidewall or (side adj w  
 S24: (2) S23 and (compress\$4)  
 S25: (0) S23 and (silicide and nitride and plug)  
 S26: (38) S23 and (silicide and nitride and plug;  
 S27: (104) ((driv\$4 or control\$4) near2 transistor) and  
 S28: (55) S27 and ((side adj wall) or sidewall or space;  
 S29: (54) S28 not (S3 S4 S5 S24 S26 S18 S19 S20)  
 S30: (53) S29 and (source and drain and substrate);

S17 and ((driv\$4 or control\$4) near2 transistor)  
 S17 and ((driv\$4 or control\$4) near2 transistor)

	U	I	PT	P	Document ID	Issue Date	Pages	Title	A	Current OR	Current
1					US 20050051772 A1	20050310	34	Semiconductor device and method of manufacturing the same	257/59	257/59	257/59
2					US 20050041505 A1	20050224	67	Ferroelectric memory and method for manufacturing the same	365/222	365/222	365/222
3					US 20040232511 A1	20041125	22	Semiconductor device and method of manufacturing the same	257/500	257/500	257/500
4					US 20040203207 A1	20041014	31	Semiconductor device and method of manufacturing the same	438/258	438/258	438/258
5					US 20040026740 A1	20040212	32	Semiconductor device and a method of manufacturing the same	257/380	257/380	257/380
6					US 20030227049 A1	20031211	31	Non-volatile semiconductor memory device	257/315	257/315	257/315
7					US 20030222294 A1	20031204	37	Nonvolatile semiconductor storage device	257/298	257/298	257/298
8					US 20030203372 A1	20031030	41	Nonvolatile semiconductor memory device and its manufacturing method	438/257	438/257	438/257
9					US 20030022422 A1	20030130	28	Semiconductor device and its manufacturing method	438/183	438/183	438/183
10					US 20020127791 A1	20020812	43	Semiconductor device and its manufacture method	438/231	438/231	438/231
11					US 20020045011 A1	20020418	70	Ferroelectric memory and method for manufacturing the same	438/240	438/240	438/240

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	1	"20040178516"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 12:36
S2	18	ogata-tamotsu.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 12:37
S3	1	"20040178516"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 16:47
S4	18	ogata-tamotsu.in.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 16:47
S5	7	S4 and transistor and (hole or open\$4) and gate and substrate	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 16:50
S6	1	"9213802"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 16:51
S12	1	"09213802"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 16:53
S13	1	"11168199"	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 16:56
S14	7374	transistor and ((interlayer near2 (insulat\$4 or dielectric)) or (interdielectric or interinsulat\$4 or inter-dielectric or inter-insulat\$4 or (inter adj (dielectric or insulati\$4)))) and (open\$4 or hole) and source and drain and gate and (sidewall or (side adj wall) or spacer)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 17:00
S15	1356	S14 and (second adj gate)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 17:00
S16	152	S15 and (second adj (sidewall or (side adj wall) or spacer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 17:01
S17	137	S16 and (conduct\$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 17:02
S18	36	S17 and ((driv\$4 or control\$4) near2 transistor)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:14
S19	3	("4305200"   "4925807"   "5061975").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2005/03/11 17:53
S20	20	("5621232").URPN.	USPAT	OR	ON	2005/03/11 17:56
S22	101	S17 not (S18 S19 S20)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:04

S23	101	S22 and (second adj (sidewall or (side adj wall) or spacer))	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:04
S24	2	S23 and (compress\$4)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:05
S25	0	S23 and (cilicide and nitride and plug)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:07
S26	38	S23 and (silicide and nitride and plug)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:14
S27	104	((driv\$4 or control\$4) near2 transistor) and (load adj transistor) and gate and ((interlayer near2 (insulat\$4 or dielectric)) or interdielectric or interinsulat\$4 or inter-dielectric or inter-insulat\$4 or (inter adj (dielectric or insulat\$4))) and plug	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:16
S28	55	S27 and ((side adj wall) or sidewall or spacer)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:17
S29	54	S28 not (S3 S4 S5 S24 S26 S18 S19 S20)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:17
S30	53	S29 and (source and drain and substrate)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:18
S31	40	S30 and gate and nitride and oxide	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:25
S32	13	S30 not S31	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2005/03/11 18:25